



Docket No.: 57454-138

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Yasuhiko TSUKIKAWA

Serial No.: 09/877,027

Filed: June 11, 2001

For: CONFIGURATION FOR GENERATING A CLOCK INCLUDING A DELAY CIRCUIT  
AND METHOD THEREOF

Group Art Unit: 2816

Examiner: Linh M. NGUYEN

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1-30-03  
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JAN 23 2003  
TECHNOLOGY CENTER 2800

**AMENDMENT UNDER 37 C.F.R. 1.111**

Assistant Commissioner for Patents  
Washington, DC 20231

Sir:

The following amendment and remarks are submitted in response to the Official Action  
mailed October 21, 2002. Please amend the application as follows.

**IN THE CLAIMS**

Please amend claims 1, 4, 11 and 14 as follows:

1. (Twice Amended) A delay locked loop comprising:

a delay circuit delaying a first clock to output a second clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for  
selectively generating one of a signal to increase an amount of delay of said delay circuit and a  
signal to decrease said amount of delay of said delay circuit;

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